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Enhanced Logic Performance with Semiconducting Bilayer Graphene Channels

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ABSTRACT Realization of logic circuits in graphene with an energy gap (EG) remains one of the main challenges for graphene electronics. We found that large transport EGs (>100 meV) can be fulfilled in dual-gated bilayer graphene underneath a simple alumina passivation top gate stack, which directly contacts the graphene channels without an inserted buffer layer. With the presence of EGs, the electrical properties of the graphene transistors are significantly enhanced, as manifested by enhanced on/off current ratio, subthreshold slope, and current saturation. For the first time, complementary-like semiconducting logic graphene inverters are demonstrated that show a large improvement over their metallic counterparts. This result may open the way for logic applications of gap-engineered graphene.

KEYWORDS: graphene · energy gap · field-effect transistor · logic gate · nanoelectronics

Since the isolation of graphene in 2004,[1] its suitability as a channel material in the postsilicon era has been an interesting but challenging topic.[2−4] Besides ultrahigh carrier mobility,[5,6] graphene also has advantages over other candidates (*e.g.*, carbon nanotubes) for nanoelectronics, such as being free of chirality and diameter control, and availability of large-area sheets.[7] However, the intrinsic metal nature and lack of energy gaps (EGs)[8] make it difficult to turn off a graphene field-effect transistor (FET) and to incorporate it into logic electronic devices. Thus, logic applications with graphene, especially with a substantial EG, are rarely explored,[9−11] despite the rapid progress in radio-frequency analog applications in recent years.[12,13] It is necessary to introduce an EG into graphene to reduce the off-state current. For this purpose, two main schemes have been proposed: lateral confinement[14−16] and inversion symmetry breaking.[17−20] In the former scheme, sizable EGs were successfully opened by cutting the graphene into ultranarrow ribbons (GNRs) and were demonstrated by high-performance GNR-FETs.[21,22] However, this also drives the channel width into a lithography inaccessible range (<10 nm) and causes large carrier-mobility degradation. In contrast, no strict dimensional limitation is imposed with the latter scheme. For instance, within perpendicular electric fields the band structure would vary considerably in bilayer graphene (BLG) sheets, which would lead to a gap between the conduction and valence bands.[23,24]

A complementary logic inverter, also known as a NOT gate, is one of the building block of integrated circuits. It consists of two FETs with opposite carrier types and is usually used as a prototype to test emerging electronic materials.[25−27] In a significant advancement,[10] Traversi and coworkers first demonstrated graphene inverters with complementary-like geometry. However, only a metallic single layer graphene (SLG) channel was used. In another work,[11] although a dual-gated BLG structure was employed, no substantial EG was observed. These initial studies also had a common limitation, that is, using thick dielectric coupling layers (300 nm SiO_2 in ref 10, and 50 nm AlO_x in ref 11), which normally requires high operation bias (input voltage, V_{IN}), and thus none were able to reach device performance with >0.05 voltage gain and >20% output voltage (V_{OUT}) swing. Three factors are essential for an inverter unit: the switching characteristics, gating efficiency, and circuitry geometry. Recently, we have been able to significantly enhance the inverter performance (*e.g.*, voltage gain of 6) in gapless SLG devices by adopting a highly efficient alumina dielectric.[28] It is anticipated that the performance would be further improved if a sizable EG could be introduced into the devices.

In this work, we report the electric properties of the first semiconducting graphene

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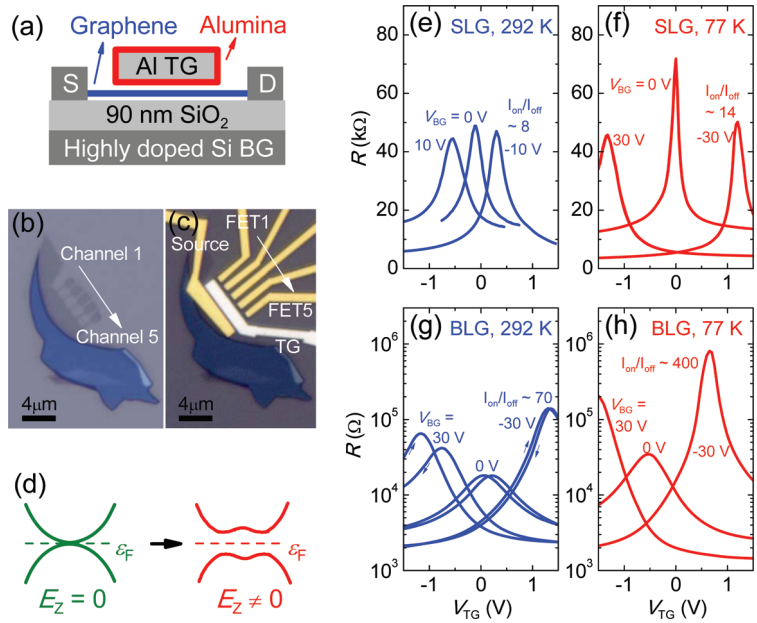

Figure 1. (a) Cross-sectional diagram of the dual-gate graphene FET. Typical optical microscopy images of a device (b) before and (c) after electrode formation. Five FETs are defined on a single graphene flake. (d) Schematic band structures for the BLG before and after application of a perpendicular electric field $\mathbf{E}_z$. (e−h) *R* characteristics for both the SLG and BLG FETs at ambient and liquid-nitrogen temperatures. A gating hysteresis arises at *RT* as shown in panel g, but it is almost eliminated at the liquid-nitrogen temperature, as shown in panel h.

logic inverters based on a buffer-free top gate dielectric method. Sufficiently strong perpendicular electric fields can be obtained under low top gate (TG) voltage ($V_{TG} < 1.5$ V), due to the high capacitive efficiency of the TG stack. We find that the alumina dielectric can effectively suppress the extrinsic charges, and a >100 meV transport EG is obtained, comparable to the state-of-art semiconducting BLG FETs,[29] in which a buffer layer, such as polymer NFC, is required to separate graphene from oxide dielectric. In contrast to the metallic SLG inverters that exhibit high performance at high supply bias (V_{DD}), the BLG devices exhibit superior electrical characteristics in the low V_{DD} region with a maximum V_{OUT} swing of 80% and a highest voltage gain of 7. The existence of the EG can greatly reduce the operating current, which promises to solve the issue of power consumption confronted by SLG inverters. Most importantly, the suitable operating V_{DD} level is around 0.5−1 V, which indicates high compatibility with the present microchip CMOS bias level and that planned for the future.[2]

RESULTS AND DISCUSSION

Although the existence of an EG in perpendicular electric field biased BLGs has been predicted by theoretical studies (Figure 1d)[17−19] and confirmed by optical experiments,[23] the expected insulating state has been elusive in transport measurements.[24] In principle, the off-state current is closely correlated to the residual carrier concentration n_0, and should ideally approach zero at the charge neutrality point (CNP) in the biased BLGs, due to disappearance of density of states.[30] However, in real devices, large charge inhomogeneity (cause electron and hole puddles at CNP) is present due to extrinsic charge sources (such as interfacial trapped charges, residing charges inside substrates, and charged adsorbates). Such scattering sources can also degrade mobility.[31,32] In this sense, to exclude the extrinsic charge sources is important not only to reduce n_0, but also to improve mobility μ. By inserting a buffer layer (polymer NFC) between the high-κ dielectric and graphene, a low n_0 of 2.8×10^{11}/cm^2 and a high room temperature (RT) μ of 7300 cm^2/(V s) have been achieved in SLG.[33] Application of the same technique to BLG resulted in an observed EG of >130 meV.[29]

In our experiment, a thin and dense natural alumina passivation layer was adopted as the TG dielectric, not only for the purpose of high gating efficiency,[28,34] but also to preserve the intrinsic behavior of graphene. It was reported that a lower n_0 of 2.3×10^{11}/cm^2 and a higher RT μ (8600 cm^2/(V s)) are observed in SLGs under a direct contact medium-κ (4.5−8.9) alumina dielectric,[35] which implies a simpler buffer-free solution to suppress the extrinsic charge sources. We identified that even without additional buffer layers, a large EG could be also achieved in our BLG samples exfoliated from natural graphite and covered with the natural alumina TG dielectric. High-purity natural graphite may contain fewer defects, and the formation of alumina dielectric by natural oxidation[34,35] may introduce fewer charge impurities compared with conventional methods. The medium permittivity of alumina leads to reduced interfacial polar phonons, which may also help to maintain the intrinsic μ. All factors are critical to the preservation of intrinsic behavior and the realization of a large transport EG.

The effect of the buffer-free alumina passivation dielectric on the graphene channels was first verified on SLG flakes. Without deducting the series resistance (R_s, from the TG uncovered graphene regions near source and drain) and the contact resistance (R_c), the maximum on/off ratio (at bottom gate voltage, $V_{BG} = -30$ V) can reach 8 and 14 at RT and 77 K, respectively (Figure 1 panels e and f). The R curves exhibit rather sharp peaks, which indicates small residual charge densities at the CNP. With consideration of the quantum capacitance, the R curves were fitted using the expression[35]

$$R_{tot} = R_c + R_s + \frac{L}{We\mu\sqrt{n_0^2 + n^2}} \quad (1)$$

where R_{tot} is the total resistance, L is the channel length, W is the channel width, and n is the gate-induced carrier density; n_0 and μ at $V_{BG} = 0$ were estimated to be 3.5×10^{11}/cm^2 and 5000 cm^2/(V s) under ambient conditions (292 k, air) and were improved to 1.4×10^{11}/cm^2 and 8500 cm^2/(V s) in liquid nitrogen (77 K), which suggests that the alumina passivation dielectric has excellent inertness toward the graphene channel, bringing a small number of extrinsic charges. Therefore, in addition to the high coupling efficiency and the simplicity in simultaneously fabricating both the TG and dielectric,[28,34] this TG stack technique also provides a buffer-free operation in preserving the intrinsic behavior of the graphene channels.

The effect of the novel dielectric was then verified on BLG flakes. Figure 1 panels g and h show the R characteristics as a function of V_{TG} (from -1.5 to 1.5 V) under different BG voltages ($V_{BG} = -30$, 0, and 30 V). Contrary to the SLG FETs in which the R peak (R_{CNP}) slightly decreases with V_{BG} (because R_s decreases when increasing V_{BG}), the R_{CNP} of the BLG FETs increased considerably with V_{BG} (more strictly, perpendicular displacement field D_z), irrespective of the measurement temperature. Such a tendency is consistent with the theoretical prediction of opening and expansion of EG with D_z.[17−19] At RT, R_{CNP} increases 7.7 times when V_{BG} is changed from 0 ($V_{TG} \approx 0$, $D_z \approx 0$) to -30 V ($V_{TG} = 1.3$ V, $D_z = 1.3$ V/nm). Assuming that the off current is dominated by the thermionic emission process through a Schottky barrier, as suggested by ref 29, a barrier variation around 52 meV can be extracted accordingly. Typically, the barrier has a maximum when the Fermi level of the contact is aligned to the middle of EG of the channel (*i.e.*, EG is twice that of the barrier). This indicates that the transport EG at $D_z = 1.3$ V/nm is at least 100 meV, which is comparable to the value obtained in ref 29, but realized under lower V_{TG} bias and a much simpler TG fabrication process. We note that the observed transport gap is still much smaller than that revealed by optical measurements (*ca.* 130 meV) under the same D_z condition, and better FET performance would be expected if the extrinsic factors in BLG could be further minimized. It should also be kept in mind that although the observed value is large for biased BLG, it is relatively small compared with conventional semiconductor materials. The estimated 52 meV barrier is also rather low with respect to the RT thermal activation energy $k_BT \approx 26$ meV and therefore is insufficient to effectively block thermal carrier injection at RT. Therefore, the EG obtained here cannot support high performance RT operation (Supporting Information for RT characteristics). To demonstrate the effect of the small EG in graphene, the following measurements were all performed in liquid nitrogen at 77 K to reduce the thermal activation energy. The nitrogen atmosphere also enables suppression of the gating hysteresis caused by oxygen and humidity desorption/absorption. Upon replacing SLG with BLG for the channel, better on/off ratios from 14 to 400 and enhanced subthreshold slopes from 600 to 160 mV/decade were obtained.

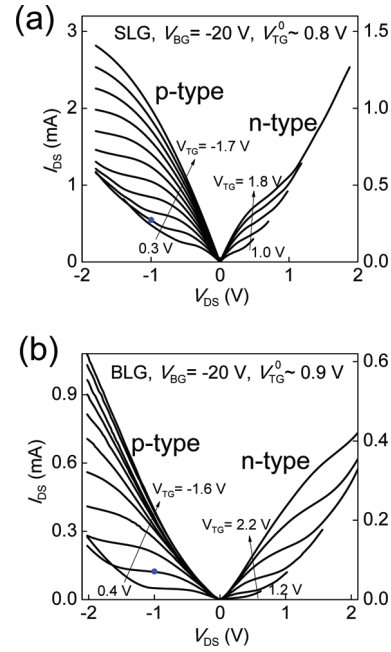

Figure 2. Output characteristics for both the (a) metallic SLG and (b) semiconducting BLG FETs at $V_{BG} = -20$ V. The left and right longitudinal axes are for the p- and n-type branches, respectively. Two solid dots indicate the bias condition of $V_{TG} - V_{TG}^0 = -0.7$ V and $V_{DS} = -1$ V.

Opening of an EG in the BLG FETs is also reflected by the different output characteristics from the SLG FETs. Figure 2 displays a series plot of $I_{DS}-V_{DS}$ curves for the both types of FETs. For the gapless SLG FETs, the unique current saturation behavior and second linear region[36] is clearly present in small $\Delta V_{TG} = |V_{TG} - V_{TG}^0|$ curves in Figure 2a, indicating the absence of barrier for minority carrier injection.[3,36] The I_{DS} curves also cross with one another when V_{DS} is sufficiently large, resulting in a zero or even negative transconductance, which implies the loss of effective control of gate on channel current. In contrast, the current saturation characteristic is largely improved in the BLG FET with the presence of EG, as reflected by the smaller slope and more extended current saturation region in Figure 2b. At $V_{TG} - V_{TG}^0 = -0.7$ V and $V_{DS} = -1$ V (indicated by solid dots), the drain conductance $g_{DS} =$

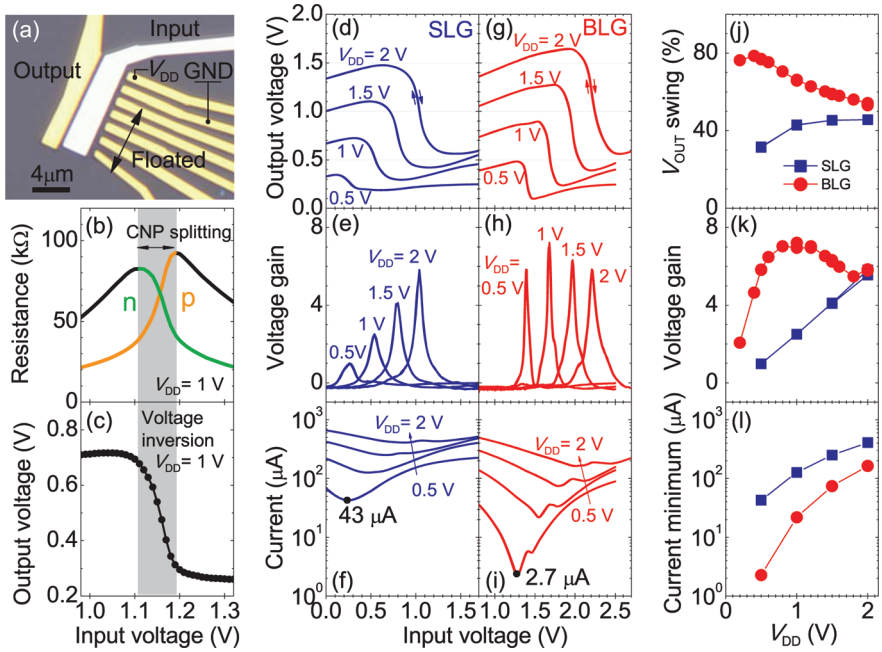

Figure 3. Operating principle and electrical characteristics for complementary-like graphene inverters. The applied V_{BG} is 0 and −30 V for the SLG and BLG inverters, respectively. In the BLG device, large V_{BG} is used to create a large EG (~100 meV) and improve device performance: (a) wiring schematic, (b) formation of CNP splitting and (c) resulting voltage inversion under V_{DD} bias in a BLG inverter; (d−l) output response, voltage gain, and normalized channel current as a function of input voltage for both the metallic SLG and semiconducting BLG devices. The V_{DD} is changed from 0.5 to 2 V in panels d−i, and from 0.2 to 2 V for the BLG device in panels j−l.

$(\partial I_{DS}/\partial V_{DS})|_{V_{TG},V_{BG}}$ values for SLG and BLG FETs are 620 and 31 μA/V, respectively, indicating a 20 times improvement of current saturation. The improved current saturation behavior may also lead to a better intrinsic gain for radio-frequency analog applications.[3]

Complementary-like semiconducting logic inverters were fabricated on the basis of the ambipolarity of graphene FETs,[28] as pictured in Figure 3a and with the operating principle shown in Figure 3b,c. The common TG and source are used as input and output electrodes, respectively. For comparison, the electrical performance characteristics of both the metallic SLG and semiconducting BLG inverters are shown in Figure 3d−i. An apparent improvement in V_{OUT} swing is observed for the BLG device in the measured V_{DD} ranges due to suppressed σ_0 (Figure 3d,g), and this trend is summarized in Figure 3j. When V_{DD} is increased from 0 to 2 V, the V_{OUT} swing (defined as $(V_{OUT}^{max} - V_{OUT}^{min})/V_{DD} \times 100\%$) increases slightly from 30 to 45% for the SLG device, while for the BLG device it has a maximum at 80% and then decreases to 55% as V_{DD} increases until 2 V. A sharper voltage inversion (especially in the low V_{DD} region) is observed when BLG channels are used, which becomes more apparent when comparing the voltage gain (defined as the maximum $-\mathrm{d}V_{OUT}/\mathrm{d}V_{IN}$) in Figure 3e,h. Specifically, the voltage gain increases by a factor of 6 (from 1 to 6) at $V_{DD} = 0.5$ V in the BLG device, which suggests that the role of the EG is significant. The voltage gain for both devices also has a different dependence on V_{DD} (Figure 3k). It is approximately linear for the SLG device, while becoming nonmonotonic with a maximum of ~7 at $V_{DD} = 1$ V for the BLG device. Furthermore, the operating current also decreases with the introduction of the EG. The current minimum is reduced by 1 order of magnitude at $V_{DD} = 0.5$ V (Figure 3l). Overall, the BLG inverter exhibits an obvious improvement of inverter performance in the low V_{DD} region with the presence of the EG. In the high V_{DD} region, the performance of the BLG device degrades to that of the SLG device.

We now qualitatively discuss the factors that determine the device performance. If R_s and R_c are neglected and a linear $\sigma - V_{TG}$ relation is assumed ($\sigma = \sigma_0 + k|V_{TG} - V_{TG}^0|$, where k is the tunability of conductance through gate voltage, σ_0 is the off-state conductance, and V_{TG}^0 is the CNP position), then the voltage gain and V_{OUT} swing can be simply expressed as (see Supporting Information for derivation)

$$V_{out}\ \text{swing} = \frac{1}{1 + 2\sigma_0/k\Delta} \quad (2)$$

$$\text{voltage gain} = \frac{V_{DD}}{2\sigma_0/k + \Delta} \quad (3)$$

where Δ is the CNP splitting between the two FETs along the V_{IN} axis. The improvement of V_{OUT} swing and voltage gain in the BLG devices in low V_{DD} regions relies on two factors: (1) high capacitive efficiency (*ca.* 920 nF/cm^2) which enables a high k value, and (2) introduction of EG which leads to a small σ_0 (or large R_{CNP}). At high V_{DD}, both the σ_0 and k decrease where extra carriers are induced at the off state,[3,36] leading to a performance degradation, as shown in Figure 3j,k. Interestingly, a large Δ value is ben-

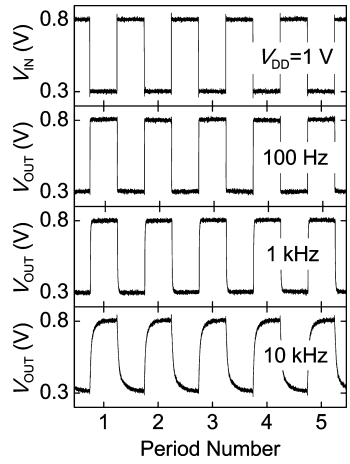

Figure 4. Logic operations for a BLG inverter at 0.1−10 kHz with V_{DD} = 1 V. The applied V_{BG} is −6 V to tune the complementary range and achieve a voltage match between input and output. The Boolean "0" and "1" are defined at 0.3 and 0.8 V, respectively.

eficial for V_{OUT} swing but unfavorable for voltage gain, and at fixed V_{DD} there is a trade-off between them.

To demonstrate the logic operations on the BLG device, dynamic response was also tested under 0.1−10 kHz square-waveform stimulus (Figure 4). Here, V_{DD} was set at 1 V and V_{BG} was selected at −6 V to match V_{IN} and V_{OUT}. Such a biasing condition leads to high and low logic voltage levels at 0.8 and 0.3 V, respectively. The ability of exhibiting matched input and output signals under a decreased V_{DD} level further reduces the power consumption with respect to a previous SLG device.[28] At frequencies of 0.1 and 1 kHz, the output response exhibits well-defined inversion behavior of the input signal, which indicates its excellent Boolean operation capability. At higher frequencies (*e.g.,* 10 kHz), small output deformation is observed that can be ascribed to the large stray capacitance of the measurement system.

In this work, the introduction of the EG into the BLG channel significantly improves the low-bias performance, with the appropriate V_{DD} region around 0.5−1 V. In particular, at V_{DD} = 0.5 V, the gain and V_{OUT} swing reach *ca.* 6 and 80%, respectively. It is important to note that the present semiconductor microchip V_{DD} criterion is 1 V and is expected to be reduced to 0.7−0.8 V in 2024 with further feature size scaling down.[2] Therefore, semiconducting graphene can satisfy the low bias requirement for future microchips. Significantly, the atomic channel thickness of graphene greatly reduces the effective vertical depletion length and helps to minimize the characteristic scale length, which may allow graphene FETs to be scaled to shorter channel lengths and higher speeds without encountering the adverse short channel effects.[3,37] In this regard, graphene may be an exclusively suitable channel material with respect to dimensionality for the postsilicon era. The present work also signifies a relatively simple fabrication technique for logic components, because it requires neither a doping process to realize the complementary geometry, nor rigorous dimensional control to create the EGs. Most importantly, it is a real lithography-compatible technique, making it superior to those integrated with nanowires or nanotubes in which the location and alignment control remain an issue. The rapid development of large-area graphene growth techniques in recent years, especially with chemical vapor deposition,[7] has further paved the way for electronic applications employing graphene. Moreover, several recent experiments, such as chemical modification[38,39] and structure perforation (graphene nanomesh)[40,41] have also showed promising results with respect to the creation of large EGs in graphene. For instance, graphene can be transformed from a highly conductive semimetal into an insulator by reversible hydrogenation.[38] In particular, a high on/off ratio of 2 orders of magnitude is observed in graphene nanomesh samples at RT.[40] These novel methods, in principle being lithography compatible, would also lend themselves to gap-engineered graphene electronics, if reasonably high carrier mobility could be retained as the EGs are opened.

CONCLUSIONS

We have demonstrated a simple and buffer-free TG dielectric technique, which is able to preserve the intrinsic nature and achieve a large transport EG in BLG. On the basis of EG, the electrical characteristics of the complementary-like semiconducting bilayer graphene logic inverters were reported for the first time. Although the EG is not sufficiently large to support high-performance RT operation, the low T results, which do show significant improvement for low-bias performance over metallic inverters, still provide a strong indication of the possibility of gapped graphene as an excellent channel material for future integrated circuits. With further advances in gap engineering, the graphene device may find applications in logic circuits.

METHODS

The graphene flakes used in this experiment were exfoliated from natural graphite. Conventional electron beam lithography and thermal evaporation (50 nm Au/5 nm Ti) were used to define the interconnection leads on devices.[28,34,42] The structures of the dual-gated FETs (Figure 1a) resemble those in previous reports,[24,36] in which a graphene sheet is sandwiched by a TG and a degenerately doped silicon bottom gate (BG, with 90-nm SiO_2 dielectric). Figure 1b,c show optical microscope images for a typical device before and after electrode formation. An array of five FET channels (FET1-FET5) were simultaneously defined with equal dimensions on a single graphene sheet. The experimental channel widths and lengths ranged from 250−350 nm and 1.2−3.6 μm, respectively. The dimension between devices may vary slightly and adapt to the sizes of exfoliated graphene flakes.

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Supporting Information Available: Reliability of top gate, detailed electrical characteristics for SLG and BLG FETs, mobility fittings with quantum capacitance, performance for BLG inverters under ambient environment, and derivation of qualitative expressions for V_{OUT} swing and voltage gain. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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